In The Specification:

Please amend paragraph beginning at line 12 of page 18 as follows:

--As shown in Figure 3, the input and output signal preservation circuit according to the present invention includes an input signal preservation unit 50 that is formed of a bias resistor R12 and a reactor L12 and is connected with an input terminal of the first stage amplification vacuum tube T6, a voltage compensation unit 55 that is formed of a load resistor R17, a second reactor L13 and a condenser C18 and is connected with an output terminal of the first stage amplification vacuum tube T6, an input signal preservation unit 53 that is formed of a bias resistor R18 and a reactor L14 and is connected with an input terminal of the second stage amplification vacuum tube T7, **and an output signal preservation unit 60 that is formed of** two load resistors R20 and R21, a first reactor L16, a second reactor L17 and a condenser C21.--

Please amend paragraph beginning at line 13 of page 24 as follows:

--As shown in Figure 5, **the input and output signal preservation circuit according to the present invention includes a first stage output signal preservation unit 140, a second stage output signal preservation unit 150, and the voltage compensation unit 143.** [[**the**]] **The** first stage output signal preservation unit 140 includes an input signal preservation unit 130 formed of a bias resistor R5 and a reactor L4 and connected with an input terminal of the first stage amplification vacuum tube T2, an amplification signal preservation unit 141 formed of a load resistor R7 and a first reactor L6 and connected with an output terminal of the first stage amplification vacuum tube T2 and an input terminal of the second stage amplification vacuum tube T3, and a voltage compensation unit 135 formed of a second reactor L5 and a condenser C7 and connected in parallel with the amplification

signal preservation unit 141.--

Please amend paragraph beginning at line 13 of page 25 as follows:

--The self-bias units [[~~131, 141 and 151~~]] **131, 142 and 152** are connected with the cathodes of the first, second and third amplification vacuum tubes T2, T3 and T4 and are formed of the resistors and condensers R6, C6; R8, C8 and R10, [[~~C10~~]] **C11**, so that a grid bias is formed at the bias resistor R5 connected with a grid side of the first stage amplification vacuum tube T2.--

Please amend paragraph beginning at line 8 of page 26 as follows:

--The amplification signal preservation unit 125 is further connected between the second stage amplification circuit and an output terminal of the third stage amplification circuit, namely, between the amplification signal preservation unit 151 of the second stage output signal preservation unit 150 and **the voltage compensation unit 155 connected with** an output terminal of the third stage amplification vacuum tube T4 and is formed of a load resistor R11 and a first reactor L9 for thereby compensating the voltage variation ratio with respect to the amplification output signal based on the amplification operation of the second stage amplification circuit and the third amplification circuit and stabilizing the bias voltages of two vacuum tubes T3 and T4.--

Please amend paragraph beginning at line 7 of page 27 as follows:

--When the DC power of the power unit 120 is supplied to the plate that is the anode terminal of the first stage amplification vacuum tube T2, a grid bias is formed at [[~~the resistor R6 of the self-bias unit 131 and~~]] the bias resistor R5 connected with the grid of the

first stage amplification vacuum tube T2, so that the first stage vacuum tube T2 amplifies the AC input signal Vi2 inputted into the grid and outputs to the plate.--

Please amend paragraph beginning at line 1 of page 28 as follows:

--At this time, the load resistor **[[~~R3~~]] R7** and the first reactor L6 of the amplification signal preservation unit 141 connected with an output terminal of the first stage amplification vacuum tube T2 operate in the same principle as the input signal preservation unit 30 of Figure 2A for thereby increasing an output resistance value with respect to the amplification output signal at the vacuum tube T2 of the first stage amplification circuit and the AC input signal of the second stage amplification vacuum tube T3 and preventing the attenuation of the amplification output signal (or AC input signal).--